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EXAMINER	
NGUYEN, TANH Q	
ART UNIT	PAPER NUMBER
2182	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/592,009	LEE ET AL.	
	Examiner	Art Unit	
	Tanh Q. Nguyen	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 December 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. In the prior office action, the oath or declaration is objected because it does not identify the mailing address of each inventor. In response, applicant submits an ADS (application data sheet) in accordance with 37 CFR 1.76 to provide the mailing address of each of the inventors. The city corresponding to the residence and mailing address of inventor Sherman Lee on the ADS does not agree with the city on the declaration. If the information on the ADS is correct, applicant needs to clearly indicate that the ADS is correct, otherwise, applicant needs to submit a new ADS.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 7-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Anderson et al. (USP 5,613,114).

4. As per claim 1, Anderson teaches a method for performing a context switch operation, comprising:

setting an index register [64, FIG. 1] on an address portion [col. 6, lines 30-32] of a state machine [60, 62, 64, 21-23, 31-33, 41-43, 51-53, FIG. 1] in a peripheral system [20, FIG. 1] to a first index value by a host computer [10, FIG. 1], the first index value indicating a first register [e.g. 21, 31, 41, 51 - FIG. 1] to be accessed;

accessing context data in the first register of the peripheral system based upon first index value [col. 8, lines 7-12];

setting the index register to a second index value by the host computer, the second index value indicating a second register [e.g. 22, 32, 42, 52 - FIG. 1] to be accessed; and

accessing context data in a second register of the peripheral system when the index register is set to the second index value [col. 8, lines 7-12], wherein the first and second registers are collocated with the peripheral system [the registers are collocated in the peripheral system 20, FIG. 1].

5. As per claim 7, Anderson teaches the registers [21-23, 31-33, 41-43, 51-53, FIG. 1] being dedicated to particular contexts - hence the first and second registers not being architected registers.

6. As per claim 8, Anderson teaches a system comprising:

a host computer [10, FIG. 1], the host computer including a microprocessor [12, FIG. 1];

a peripheral system [20, FIG. 1] coupled to the host computer, the peripheral system including a state machine [60, 62, 64, 21-23, 31-33, 41-43, 51-53, FIG. 1] including an index register [64, FIG. 1], the peripheral system further including a first

register [e.g. 21, 31, 41, 51 - FIG. 1] and a second register [e.g. 22, 32, 42, 52 - FIG. 1], the first register being associated with a first index value and the second register being associated with a second index value, wherein the first and second registers are collocated with the peripheral system (see rejection of claim 1 above).

an interface [29, FIG. 1] coupled to the host computer and to the peripheral system, the interface being configured to provide first and second index values from the host computer to the peripheral system; and

a register access circuit [76, 78 - FIG. 2] in the peripheral system, the register access circuit being configured to access context data in the first register when the first index value is provided by the host computer and set by a thread scheduling unit [74, FIG. 2], wherein the index register is configured to stored the first index value or the second index value, the register access circuit being further configured to access context data in the second register when the second index value is provided by the host computer and set by the thread scheduling unit. Note that "when the first index value is provided by the host computer" and "when the second index value is provided by the host computer" are not specific enough to preclude Anderson from teaching such limitation.

7. As per claim 9, see the rejection of claim 7 above.

8. As per claim 10, Anderson teaches the peripheral system including a state machine module that includes an address portion, a control portion, and a data portion (context switching unit inherently comprising address portion, control portion and data portion), the data portion including the first and second registers (see rejection of claim

8 above).

9. As per claims 11-13, Anderson teaches the peripheral system including a microprocessor [60, 62 - FIG. 1];

the address portion comprising the register access circuit [76, 78 - FIG. 2];

the peripheral system including a plurality of context registers, wherein each of the plurality of context registers is associated with one of a plurality of index values other than the first and second index values [...23-53, FIG. 1].

10. Claims 8-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Takeda (US 6,292,851).

11. As per claim 8, Takeda teaches a system comprising:

a host computer [4, FIG. 1], the host computer including a microprocessor [12, FIG. 1];

at least one peripheral system [6, FIG. 1; col. 3, lines 12-22] coupled to the host computer, the peripheral system including a state machine [6, FIG. 1; see definition of Finite state machine in Wikipedia cited in PTO-892] including an index register [26, FIG. 1], the peripheral system further including a first register [18 of one LSI 17 - FIG. 1 (col. 3, lines 40-42); register in SDRAM 32 - FIG. 2 corresponding to register 18 of the one LSI 17 (col. 5, lines 50-54] and a second register [18 of another LSI 17 - FIG. 1 (col. 3, lines 39-42); register in SDRAM 32 - FIG. 2 corresponding to register 18 of the another LSI 17 (col. 5, lines 50-54)], the first register being associated with a first index value and the second register being associated with a second index value [col. 5, lines 44-47; col. 5, lines 50-60], wherein the first and second registers are collocated with the

peripheral system (register 18 of one LSI 17; register 18 of the another LSI 17; and corresponding registers in SDRAM 32 are collocated on peripheral system 6);

an interface [8, FIG. 1] coupled to the host computer and to the peripheral system, the interface being configured to provide first and second index values from the host computer to the peripheral system [col. 5, lines 44-47]; and

a register access circuit [20, 22, 24, 34 - FIG. 2] in the peripheral system, the register access circuit being configured to access context data in the first register when the first index value is provided by the host computer (e.g. when an address provided by the host computer is associated with register 18 of one LSI 17, data in SDRAM associated with register 18 of one LSI 17, or data in register 18 of one LSI 17 are accessed), wherein the index register is configured to stored either of the first index value or the second index value (the address register is used to store an address associated with register 18 of the one LSI 17, or an address associated with register 18 of the another LSI 17), the register access circuit being further configured to access context data in the second register when the second index value is provided by the host computer (e.g. when an address provided by the host computer is associated with register 18 of the another LSI 17, data in SDRAM associated with register 18 of the another LSI 17, or data in register 18 of the another LSI 17 are accessed).

12. As per claim 9, Takeda teaches the registers not being architected registers [register 18 of the one LSI 17, register 18 of the another LSI 17, registers in SDRAM corresponding to the one LSI 17 and the another LSI 17 are dedicated to particular context - hence are not architected registers].

13. As per claim 10, Takeda teaches the peripheral system including a state machine module [6, FIG. 1] that includes an address portion [26, FIG. 1; 36, FIG. 2], a control portion [22, 30, 34, 40 - FIG. 2], and a data portion [18, 19, 28 - FIG. 1; 32, 38 - FIG. 2], the data portion including the first and second registers (see rejection of claim 8 above).

14. As per claims 11-13, Takeda teaches the peripheral system including a microprocessor [22, FIG. 1];

the address portion comprising the register access circuit [col. 5, lines 44-47];

the peripheral system including a plurality of context registers, wherein each of the plurality of context registers is associated with one of a plurality of index values other than the first and second index values [col. 3, lines 39-42].

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

17. Claims 2-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson et al..

18. As per claim 2, Anderson does not teach context data including a device address for a network device, a class value, a clock offset value and an active member address. Such context data are traditionally associated with communications in a Bluetooth environment.

Anderson in essence teaches reducing or eliminating the need for context save and restore when performing context switch operations - by using register sets, each of which being dedicated to a particular context [col. 4, lines 24-36]. Anderson, however, does not teach a Bluetooth environment.

Since it was known in the art at the time the invention was made that traditional context switch operations in a Bluetooth environment require substantial context save and restore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate registers, each of which being dedicated to a particular context (as is taught by Anderson) in a Bluetooth environment - in order to reduce and/or eliminate context save and restore when performing context switch operations in such environment (hence context data in such environment including a device address for a network device, a class value, a clock offset value and an active member address).

19. As per claims 3-6, Anderson teaches each register being dedicated to a thread,

hence teaches accessing context data comprising receiving by the peripheral system an address value that identifies an address within the register, control input identifying read/write functions, and data value to write the data value to the register for a write function, or to provide the contents of the register to the host computer for a read function - as read/write threads are known to include address, read/write functions and data value for read/write functions.

Examiner's note: *Examiner has cited particular page, column and line number(s) in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. Applicant needs to consider the references in their entirety as potentially teaching all or part of the claimed invention.*

In the case of amending the claimed invention, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and verification of the metes and bounds of the claimed invention.

Double Patenting

20. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422

F.2d 438, 164 USPQ 619 (CCPA 1970); and In *re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

21. Claims 1-13 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 4-5 of copending Application No. 11/314,036 in view of Maupin.

As per claims 1, 8, 13, claims 1, 5 of the copending application claim all the limitations of the claims except for a context index register for setting the index values. Maupin teaches a context index register for setting a value identifying a new context in a context switch operation. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a context index register, as is taught by Maupin, in order to identify a new context in a context switch operation.

As per claims 2-6, claim 5 of the copending application claims a Bluetooth network and communications in a Bluetooth network, hence the context data of claim 2, and accessing the context data of claims 3-6.

As per claims 7, 9, claim 4 of the copending application claims non-architected registers.

As per claims 10-12, claim 5 of the copending application claims a host controller, hence a state machine, a microprocessor and a register access circuit in the host controller.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Response to Arguments

22. Applicant's arguments filed October 25, 2007 with respect to the 102 and 103 rejections with Anderson have been fully considered but they are not persuasive.

Applicant appears to argue that Anderson does not teach **verbatim** "setting an index register on an address portion of a state machine" because applicant does not agree that elements 60, 62, 64, 21-23, 31-33, 41-43, 51-53 constitute a state machine and because applicant does not agree that the citation by the examiner (col. 6, lines 30-32) discloses an index register on an address portion of the state machine.

The argument with respect to the state machine is not persuasive because a state machine is by definition a model of behavior composed of a finite number of states, transitions between those states, and actions (see Finite state machine definition in Wikipedia cited in PTO-892). Since elements 60, 62, 64, 21-23, 31-33, 41-43, 51-53 constitute a model of behavior composed of a number of states (registers storing state values), transitions between those states, and actions, such elements constitute a state machine. The argument is also not persuasive because the examiner notes that applicant's disclosure shows a state machine 940 [FIGs. 7-8] with elements that are **functionally very similar** to the elements 60, 62, 64, 21-23, 31-33, 41-43, 51-53 of Anderson.

The argument with respect to an index register on an address portion of the state

machine is not persuasive because the citation by the examiner discloses a thread ID that can be decoded to provide the location of the corresponding thread. The Current Thread ID register [64, FIG. 1] stores a thread ID that can provide the **address** (location) of the corresponding thread - hence the Current Thread ID register being on an address portion of the state machine (see also argument with respect to state machine above).

23. Applicant's arguments with respect to the 103 rejections of claims 8-13 over Maupin have been considered but are moot in view of the new ground(s) of rejection by Takeda, the new ground(s) of rejection being necessitated by amendment.

24. Applicant's arguments with respect to the double patenting rejections of claims 1-13 have been considered but are moot because a terminal disclaimer has not been filed.

Conclusion

25. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

26. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tanh Q. Nguyen whose telephone number is 571-272-4154. The examiner can normally be reached on M-F 9:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on 571-272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TQN
December 12, 2007

TANH Q NGUYEN
PRIMARY EXAMINER
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12/12/07